User-friendly design approach for analog layout design

Yongfu Li, Zhao Chuan Lee, Vikas Tripathi, Valerio Perez, Yoong Seang Ong, et al.
User-Friendly Design Approach for Analog Layout Design

Yongfu Li, Zhao Chuan Lee, Vikas Tripathi, Valerio Perez, Jonathan Yoong, Seang Ong, and Colin Chiu Wing Hui

GLOBALFOUNDRIES Singapore Pte. Ltd., 60 Woodlands Industrial Park D Street 2, Singapore.

ABSTRACT

Analog circuits are sensitive to the changes in the layout environment conditions, manufacturing processes, and variations. This paper presents analog verification flow with five types of analog-focused layout constraint checks to assist engineers in identifying any potential device mismatch and layout drawing mistakes. Compared to several solutions, our approach only requires layout design, which is sufficient to recognize all the matched devices. Our approach simplifies the data preparation and allows seamless integration into the layout environment with minimum disruption to the custom layout flow. Our user-friendly analog verification flow provides the engineer with more confidence with their layout’s quality.

Keywords: Design-For-Manufacturability, Analog Layout, Circuit Design, Analog Design Rules, Litho-Friendly Design

1. INTRODUCTION

The rapid development of Internet of Things (IoT) technologies for home, retail, automotive, manufacturing and wearables applications, causes companies to face unique challenges and to accelerate their design cycle to meet the market demands. In parallel, the semiconductor industry continuously introduces more sophisticated fabrication processes to manufacture multiple devices’ variants in a single SoC design with lower power consumption and higher performances. With the unprecedented challenges faced by the circuit designers and the increasing functional requirement for the system-on-chips (SoC), the analog design has become the main bottleneck in the design process.

Traditionally, the analog circuit designers and layout engineers adopt custom circuit design techniques because the circuits are particularly sensitive to the changes in the layout environment conditions, manufacturing processes and variations. As the engineers are advancing into advanced process technology, such design techniques and practices do not guarantee that all the circuit are fully functional with its first silicon measurement. Engineers can no longer depend on their experience with proven concepts and components to design the product with the new technology.

In this paper, we implement an analog device matching check (ADMC) verification software based on the Calibre Programmable Electrical Rule Check Logic Driven Layout (PERC-LDL) industry tool,
which automatically recognize all matched devices from the layout and applies analog-focused layout constraint check to highlight any potential physical and electrical device mismatch. Compared to other works, our approach only requires the custom layout, which greatly simplifies the data preparation work, providing minimum disruption to existing custom layout flow. Therefore, our solution will address layout concerns faced by analog designers and providing them with more confident with their layout’s quality.

The rest of this paper is organized as follows. Section 2 reviews the existing works and presents the remaining challenges faced in the development of logic-aware physical verification for analog circuits. Section 3 presents our approach in improving the analog circuit verification works. Finally, in Section 4, we analyse several analog circuit layouts and present the analog constraints implemented in this work. Conclusions are given in Section 5.

2. PROBLEM STATEMENTS

Synthesizable analog layouts have been a well-studied discipline by many researchers over the years, evolving from the limited knowledge-based methods to the computational intensive optimization-based methods. The solution offers a significant paradigm shift in the custom analog design flow, but its possible adoption by the industry remains unclear. Because the quality of the synthesized layout is highly dependent on the algorithm, cost function, analog design constraints. Therefore, it is important to have a well-established analog constraint check to determine the quality of synthesized or custom drew layout.

In this section, we will discuss several possible solutions to implement the analog constraint check and its respective trade-offs. We present our implementation of a layout-driven logic-aware physical verification for analog layouts. In this paper, we focus in the area of analog constraint checks. Our goal is to implement analog-focused layout constraint check on the matched devices with minimum disruption to the existing custom layout flow.

2.1 Extending Physical Verification - Design Rule Checking

Design Rule Checking (DRC) is a physical verification method where it identifies layout locations which do not compliant to physical constraints specified by the foundry. It is possible to extend the verification method for analog layout constraints but with several prerequisites and limitations. The layout designer must place several types of marker layers to differentiate the different types of matched devices. Additional marker layer is also required to place on the nets to check net-related analog constraints. A modification of the marker layers is required whenever there is a layout correction. This technique is highly prone to error and omission. Since this technique lacks logical connectivity, it is hard to debug and understand the logical and performance impact for the new corrections.

2.2 Extending Logical Verification - Layout Versus Schematic

Layout Versus Schematic (LVS) is a logical verification method where it extracts layout netlist and reports the discrepancy between the schematic netlist and the layout netlist. Generally, LVS only reports an error when there is a discrepancy in the device’s width and length or logical connectivity. It
is possible to extend the verification method to identify additional discrepancies in the device parameters between the schematic and the layout, such as source and drain diffusion overhang (SA and SB). To differentiate the analog and digital circuit domains in the layout, designers can either use multiple transistor models to separate the analog and digital circuit or to use a marker layer in the layout to isolate the analog domains. Any modification in the marker layer is required whenever there is a layout correction and this technique is highly prone to error and omission. Since this technique provides limited physical information about the layout, it cannot provide a fully comprehensive analog constraint check.4

2.3 Combining Logical and Physical Verifications - Programmable Electrical Rule Check

PERC leverages on the logical connectivity information from the LVS check and physical information from the DRC check to perform advanced ERC, Electrostatic Discharge (ESD), Electrical Overstress (EOS), voltage-domain checks. In this work, we have extended the capability of the PERC verification method to implement our analog layout constraints.

Meyer zu Bexten5 presented the analog constraints check using the Calibre PERC to verify the compliance of a custom-designed analog layout. The engineer needs to provide the layout, schematic netlist and a list of matched devices’ constraints. The procedure is divided into two phases, namely constraint derivation and constraint verification. During the constraint derivation process, constraint list will be further refined to avoid false recognition. Transistors will unequal gate width and length will be filtered out from the constraint list. Therefore, the engineer needs to ensure that the layout passes the LVS check before executing the program, or else any matched device with unintended layout mistake with the transistors’ parameter will be filtered out.

3. OUR APPROACH - EXTENDING PROGRAMMABLE ELECTRICAL RULE CHECK

Our ADMC verification flow is built upon the foundation of the Calibre PERC-LDL industrial tool. It analyses layout using layout-aware and logic-aware analysis technique and provides an integration path for result visualization and error reporting.4 The advantages of using industry tool allow rapid software development with hyper-threading feature and GUI interface.

In this work, we built-in capability in the Calibre PERC-LDL to automatically recognise all matched devices from the layout and applies analog-focused layout constraints to highlight any potential physical and electrical device mismatch. This methodology only requires the physical layout, greatly simplifies the data preparation work and minimizes the disruption to the existing custom layout flow. As shown in Fig. 1, the verification flow is seamlessly integrated into the layout environment and is broken down into five phases.

1. Data preparation
2. Layout netlist extraction
3. Layout topology extraction
4. Layout constraint checks

5. Layout debugging process

3.1 Data preparation

One of our key innovation is to simplify the existing work by reducing the amount of data preparation work and input prerequisites. Our verification method only requires engineer to provide the customer layout. We provide an optional feature where engineers can highlight the region in the physical layout where ADMC checks are required. Unlike the DRC check, a single marker layer is sufficient in our methodology because Calibre PERC-LDL-DRC is capable of performing both layout-aware logical analysis and logic-aware analysis. Furthermore, the use of marker allows engineers to execute the checks at localized area, which significantly reduce the execution runtime and computational resources. With the use marker layer, engineers do not need to specify and classify the analog constraints.

3.2 Layout Netlist & Topology Extraction

The main challenge in analog constraint check to reduce the probability of false violation constraint checks on the unintended matched devices. As shown in Figs. 2, the differential pair topology can appear in both analog circuits (Fig. 2(a)) and digital combinations logics (Fig. 2(b)). Similarly, the cross-coupled pair topology can also appear in both analog circuits (Fig. 2(a)) and digital sequential logics (Fig. 2(c)).

To address the challenge, our approach is to derive the circuit netlist without the schematic information. We use the foundry provided LVS rule check to extract netlist from the physical layout and performs topology extraction on the netlist based on the logical topology constraints to identify the
matched devices. For the field-effect and bipolar junction transistors, the logical topology constraints are based on the common analog circuit connection referenced in the work. Since the passive devices, such as capacitor and resistor, have two terminals, the logical topology constraints are generalized with a matched device with only one common terminal.

Another key proposition of our work is to provide minimum disruption to existing custom layout flow. As such, it is not required to have an entirely LVS clean during the layout development phase, engineers can execute the ADMC and the verification result is still valid as long as the matched devices are connected correctly. Therefore, our methodology allows engineers to have an early assessment of the analog layout before the final sign-off stage.

3.3 Layout Constraint Checks

After layout topology extraction process, analog-focused layout constraint checks are applied to these identified matched devices in the layout to highlight any potential physical and electrical device mismatch. These checks are generalized and discussed in detail with examples in Section 4.

3.4 Debugging Process

The Calibre PERC-LDL framework serves as a database server, allowing physical analysis results and the optimized layout information to be stored in the Calibre Result Database (RDB) and the Calibre DFM database, respectively. The extracted logical netlist information from the optimized layout is stored separately in the Calibre Standard Verification Database (SVDB) to enable schematic visualization and inspection. During the debugging process, the result can be viewed and traversed with the Calibre standard result viewing environment (RVE), that allows engineers the ability to cross reference results for visualization and error reporting. Engineers are able to perform additional physical and logical analysis on the matched devices through the Calibre Yieldserver. Fig. 3 illustrates the Calibre LDL framework using the Calibre RVE interface where all the databases can be accessed simultaneously.

4. ANALOG DESIGN CONSTRAINTS WITH SEVERAL DESIGN USE CASES

<table>
<thead>
<tr>
<th>Item</th>
<th>Design type</th>
<th>Size (µm × µm)</th>
<th>Devices (T,C,R)</th>
<th>Topology types</th>
<th>Time (Sec)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Comparator</td>
<td>20×20</td>
<td>24,0,0</td>
<td>dp,cm</td>
<td>43</td>
</tr>
<tr>
<td>2</td>
<td>Oscillator/Timer</td>
<td>20×200</td>
<td>352,0,0</td>
<td>cp,cm</td>
<td>54</td>
</tr>
<tr>
<td>3</td>
<td>Voltage Regulator</td>
<td>60×80</td>
<td>114,0,26</td>
<td>dp,cp,cm</td>
<td>67</td>
</tr>
<tr>
<td>4</td>
<td>Phase-Locked Loop</td>
<td>400×500</td>
<td>529,16,16</td>
<td>cp,cc,cm,dp,ls, vr-II</td>
<td>279</td>
</tr>
</tbody>
</table>

- T: Transistor, C: Capacitor, R: Resistor
- dp: differential Pair, cm: current mirror, cp: cascode Pair, cc: cross-coupled Pair, ls: level-shifter, vr-II: voltage reference

---

Downloaded From: https://www.spiedigitallibrary.org/conference-proceedings-of-spie on 5/30/2018 Terms of Use: https://www.spiedigitallibrary.org/terms-of-use
Figure 2: Handling expected failure.
Figure 3: An example of Calibre RVE showing the Calibre LDL verification framework, where all the databases can be accessed simultaneously.

In our experiment, we have implemented the software using the Calibre Tcl Verification Format (TVF) programming language. We executed the program on our Linux workstation platform with Intel 2.7-GHz 8 Core Duo CPU and with 128-GB memory. The experiment was carried out on four sets of analog circuit layouts implemented in 55-nm technology, as listed in the Table 1. The metric used to study the circuit complexity, such as device count, size of the layout, type of circuit topology. The run-time refers to the total compute time taken for the verification. Our most complex analog circuit is the phase-locked loop, which occupy an area of $400\mu m \times 500\mu m$ and contains transistor, capacitor and resistor devices. The verification completes within a reasonable runtime of 5 minutes. Our software is able to identify all the matched pair devices and the corresponding constraints violation.
We discuss the details of the five different types of analog constraints implemented in the following section, namely:

1. Matched Device Parameters Constraints
2. Process Gradient Constraints
3. Dummy Constraints
4. Foreign Object Constraints
5. Device Symmetry Constraints

4.1 Matched Device Parameters Constraints

The physical properties of the matched devices are extracted and stored in the Calibre RDB database, matchedPair.rdb. As shown in Fig. 3, our database contains different type of device information such as device type, orientation, substrate/well, length, width and area. Mismatched information is derived from the matchedPair.rdb database based on the matched device parameters constraints and results are stored in a separate Calibre RDB database, admc.rdb for better data management. The matched device parameters constraints are classified into two broad categories: generic and technology-specific matching constraints.

The generic matching constraints help to identify physical mismatch for all the matched devices. As shown in Figs. 4, the error markers indicate that there are physical mismatches among the matched-pair transistors. Figs. 4(a) and (b) show that the ‘red’ error markers highlight on the transistors with the mismatched width and length, respectively. Fig. 4(c) shows that the ‘red’ error markers highlight on the transistors due to different device type, thin-oxide, thick-oxide p-type transistors. In our use case, the matched-pair transistors’ width and length are drawn with 2.00 µm and 1.00 µm except the mismatched transistors.

The technology-specific constraints help to identify physical mismatch characterized by the process technology. For example, error markers are asserted on the transistors where it fails to meet the recommended minimum length, width, area and maximum number of fingers. This is to ensure that transistors achieve a reasonable small standard deviation error for good device matching.

4.2 Process Gradient Constraints

Process gradient constraints help to identify electrical device mismatch due to variations arise over a long interaction distance between the matched devices. For example, the CMP process over a dense metal region will induces a severe dishing, causing non-uniform metal thickness on the matched devices. In particular, non-uniform metal thickness will affects the precision of the metal-oxide-metal (MOM) capacitors and thus, limiting the effective linearity and resolution of the digital-to-analog converters and the analog-to-digital converters. Special placement techniques such common centroid layout or interdigitated layout are essential to minimize the mismatched in the capacitive array and resistor ladder. It is reported that distances greater than 50 µm will adversely affect the accuracy of precise resistive or capacitance arrays. As shown in Fig. 5, the ‘blue’ error marker highlights on the region of the matched resistors because the total array width has exceeded 50 µm distance. The check allows layout engineers to further optimize the layout to minimize mismatch variations.
Figure 4: Examples of mismatched transistors’ (a) width, (b) length and (c) device type due to generic matching constraints.

4.3 Dummy Constraints

Dummy constraints help to identify device mismatch due to neighbouring layout variations. Dummy devices are placed around the matched device array so that the matched devices have the same physical surrounding environment, which ensure devices achieve the same optical proximity correction effects, channel stress effects, orientation effects and parasitic effects. As shown in Figs. 5(b), the error marker highlights the boundary of matched devices and reveals that there is an absent of dummy resistors at the left side of the resistor ladder.
4.4 Foreign Object Constraints

Foreign object constraints help to identify any unrelated physical objects within and around the matched devices. Unrelated objects such as metal routings or floating metals affect the matched devices’ proximity correction effects, parasitic effects and degrade its differential pair’s signal integrity. For example, as shown in Fig. 6(a), although the intend of the floating metals above the transistors’ region is to prevent any metal fill by foundry, these floating metals might degrade its differential pair’s signal integrity. As shown in Fig. 6(b), the constraint check highlights an unintended metal drawn between the current mirror matched pair and dummy devices. This float metal affects the proximity correction effect of the adjacent device compared to the remaining matched devices.

4.5 Device Symmetry Constraints

Device symmetry constraints help to identify physical mismatch due to asymmetry layout drawing. In the context of this paper, asymmetry layout drawing refers to unequal drawing for poly-poly spacing, poly-contact spacing, source and drain diffusion overhang and poly extension from diffusion. Therefore, any asymmetry layout drawings will adversely affect the matched devices. For example, as shown in Fig. 7, the constraint check reported two different values of the contact and the polygon spacing, which results in a difference between the source-gate and drain-gate resistances.
Figure 6: (a) The ‘red’ error markers highlight the floating metals, which are drawn above the transistors’ region and induce charges to the differential pair (b). The ‘red’ error markers highlight the floating metals between the current mirror matched pair and dummy devices.

5. CONCLUSION

In this work, we present an innovative software solution to address analog layout quality concerns faced by the analog designers. Our software requires only the layout, thus simplifies the data preparation and allows seamless integration into the layout environment with minimum disruption to the custom layout flow. The verification can be done incrementally and does not required a completely clean LVS, which assists the layout engineers to quickly access and identify their drawing mistakes during the development phase. Hence, our user-friendly verification flow reduces the verification time during the LVS sign-offs and provides engineers with more confident with their layout’s quality. In our future work, we will incorporate lithography friendly analog constraint checks such as color de-
Figure 7: The measurements between the contact to the poly layers indicate 2 different spacing values, 82nm and 90nm, which are reported as a constraint check in the Calibre RDB database.

composition check on matched devices.

ACKNOWLEDGMENTS

The authors would like to special thanks Shitiz Arora for co-implementing the software.

REFERENCES


