A 2.89-µW Clockless Fully-Integrated Wireless ECG SoC for Wearable Sensors

ABSTRACT
A wireless electrocardiogram system-on-chip based on event-driven system architecture is demonstrated. An analog-to-information converter enables 10 times reduction in sampling points. A DC-input analog front-end with baseline stabilizer minimizes motion artifacts in wearable applications. Implemented in 0.13 µm CMOS technology, the entire system consumes 2.89 µW under 1.2 V supply when transmitting raw ECG data.

Categories and Subject Descriptors
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General Terms
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Keywords
ECG, event-driven, level-crossing ADC, analog front-end, analog-to-information converter, ultra-wideband, System-on-Chip.

1. INTRODUCTION
Cardiovascular disease is the leading cause of death around the world. Over half of people aged 50 and above suffer from some forms of arrhythmia, such as palpitations, atrial fibrillation and syncope. Individuals with atrial fibrillation have a risk of stroke that is 3 to 5 times greater than those without atrial fibrillation [1]. The diagnosis of arrhythmia is traditionally carried out by a portable electrocardiogram (ECG) device, such as Holter that lasts for one to three days. Studies show that long-term ambulatory ECG monitoring significantly improves diagnostic yield in arrhythmia. Compared to the Holter, the wearable ECG patch with wireless connection to a smart phone is capable of capturing even the very infrequent arrhythmias during normal daily activities, and make early diagnosis possible by sending the data to cardiologists in real time. It also helps patients to manage stroke risk.

A non-intrusive wireless wearable ECG sensor is an ideal solution to achieve long term ambulatory ECG monitoring. However, the design of such sensor is extremely challenging. The available power source from embedded batteries is highly limited, due to its patch-like size and light weight. For example, using an ultralight lithium thin film battery of size 25.7×25.7 mm² with thickness of 220 µm and capacity of 700 µAh at 3.9 V, the entire circuit power must be less than 3.3 µW if aiming for 7-day use, assuming a power efficiency of 80 %. On the other hand, wireless function is essential for data transmission, and the radio often consumes significant power. Therefore, the key challenge for long-term operation is to minimize the power of wireless transmitter (TX). Moreover, it is desirable if the sensor is capable of recording ECG signals from dry electrodes instead of traditional wet electrodes, which avoids skin itching and saves the hassle of frequently changing the electrodes. In addition, a higher level of integration with fewer external components helps reduce cost and makes flexible sensor possible.

This paper reports an ultra low-power clockless wireless ECG system-on-chip (SoC) for wearable ECG patches. It adopts the event-driven architecture to reduce the data rate and eliminate the need of clock thus significantly lowering the power of overall chip. A DC-input high-impedance analog front-end (AFE) with baseline stabilizer is proposed to enhance signal quality for long-term use. The antenna is embedded on chip to minimize the off-chip components, which makes it easy to attach the chip to a flexible substrate. The on-chip antenna works well for our intended application, in which an ECG patch is pasted on the chest and the wireless receiver (RX) is kept in a T-shirt pocket that covers the ECG patch. Under such scenario, the communication distance between the patch and the wireless receiver is within few centimeters, which justifies for an on-chip antenna.

The paper is organized as follows. After Introduction, Section 2 introduces the SoC architecture, design considerations, and the event-driven analog-to-information (A2I) converter. The circuit implementation in Section 3 covers the DC-input high-impedance front-end with baseline stabilizer, the level-crossing ADC in A2I, the pulse encoder and the UWB transmitter. We provide measurement setup and experimental results in Section 4, followed by the conclusion in Section 5.
2. SYSTEM OVERVIEW
To achieve the design target of less than 3.3 µW discussed in Section 1, the sensor architecture must be carefully chosen. It is well known that the wireless block is often the most power consuming part in a biomedical sensor [2]. Thus, it is rewarding to optimize the power of wireless block. The low-power radio design techniques, lossless data compression, signal feature extraction, aggressive duty-cycling of radio are some of the available tools for power reduction [3]. However, none of them could lead to a solution that meets the target power of 3.3 µW. Lossless data compression, which is necessary for biomedical signals, provides limited compression ratio [4]. Feature extraction significantly minimizes the data volume, but fails to provide raw data that is required by most of clinicians. Heavy duty-cycling needs the support of large memory block, which consumes both area and power. The system architecture presented in this paper is a departure from traditional signal flow, where analog signal is converted into digital signal and transmitted by a radio. The proposed architecture keeps input signal in analog form throughout the signal chain, leading to a clockless event-driven system architecture, as shown in Fig. 1.

The system consists of an analog front-end (AFE), an analog-to-information converter (A2I), a 1B2B pulse encoder, and an impulse-radio ultra wideband (IR-UWB) transmitter. The ECG signal is first amplified by the low-noise analog front-end, and then transformed to a pulse train in an A2I converter. The A2I includes a level-crossing (LC) analog-to-digital converter (ADC) with 32 quantization levels, which is sufficient for recording ECG signal according to the study in [5]. A QRS detector could be embedded into the LC-ADC using the algorithms presented in [6] if on-chip heart-rate detection is needed. We did not include a QRS detector in this design because the transmission of raw ECG data or QRS does not make large differences in power consumption. In fact, the average data rate for raw ECG is around 25 Hz, which is similar to the findings in [5]. The low data rate allows us to turn off UWB transmitter in between the pulses, resulting excellent power efficiency. The A2I output, in the form of two pulse trains, is fed into 1B2B pulse encoder to generate a single pulse stream for wireless transmission. The pulse stream is sent to a gateway device, i.e., in the T-shirt pocket of a patient, by the IR-UWB transmitter which integrates with an on-chip antenna. The combination of the A2I and IR-UWB removes the clock in the system, which makes the entire system intrinsically duty-cycled based on input events.

3. CIRCUIT IMPLEMENTATION

To maximize the output dynamic and TX output swing, the supply of 1.2 V is used. Given the 3.3 µW power budget, the available total current is less than 2.8 µA, which is divided among the AFE, A2I ADC, 1B2B encoder. This section discusses the circuit implementation of those blocks, with main focuses on the low-power techniques to achieve the power requirement without compromising the major sensor functions.

3.1 DC-Input Instrumental Amplifier

In ambulatory ECG recording, the motion artifacts, associated with the sudden changes of skin-electrode impedance, greatly affect signal quality. Severe motion artifacts could destroy the diagnosis value of ECG signal. An effective way to mitigate motion artifacts is to increase input impedance, which reduces the loading effects caused by the skin-electrode interface. The way to achieve high input impedance is to minimize capacitance or resistance on the input port. This can be done by either DC-coupling or impedance boost circuit. We choose DC-coupling for its simplicity and low power implementation.

The proposed DC-input AFE is shown in Fig. 2. The inputs $V_{IN+}$, $V_{IN-}$ from electrodes are directly connected to the gate of the transistors in the two instrumental amplifiers (IAs). The parasitic $C_p$ becomes the main factor affecting the input impedance. Without choppers or large capacitors connected to the input, up to $G\Omega$ impedance in ECG frequencies are
3.2 Baseline Stabilizer

First, DC attenuation is provided by the IA stage, highlighted in the gray box in Fig. 2, as well as the subsequent programmable-gain amplifier (PGA). Based on the transfer function of the IA

\[
\frac{V_o}{V_{IN}} = \frac{1 + j\omega \cdot 50R_1C_1}{1 + j\omega \cdot R_1C_1}
\]  

the amplifier DC gain is 1, compared to the AC gain at ECG frequencies of 50. Therefore at the IA output, the desired ECG signal is amplified while the DC offset stays with the same amplitude. Effectively the DC offset is attenuated relative to the ECG signal. After this 50 x attenuation, the ECG signal is further amplified by the AC-coupling PGA, with tunable gain from 1.5 to 12 by adjusting the ratio of \(C_{28}\). Because the input impedance is no longer an issue at the input of the PGA, the PGA stage adopts AC-coupling to block the residual DC offset completely.

Second, to avoid input DC drifting away from the designed input DC range, two resistors (\(R_0\)) are introduced between two input ports to stabilize DC with the midpoint connected to common mode voltage. In addition to stabilize DC, \(R_0\) together with \(C_p\) serves as a high-pass filter. Since \(C_p\) is around 1 pF, \(R_0\) must be over 100 GΩ to achieve a cut-off frequency of less than 0.05 Hz as required by ECG recording standard. \(R_0\) is implemented using thick-oxide PMOS pseudo resistor [8]. With such a large resistance, the introduction of \(R_0\) does not affect the ECG amplitude or cause impedance degradation.

The noise performance of the AFE often determines the entire sensor’s noise floor. Therefore, adequate power must be allocated to the AFE and in particular the IA stage. Given the 2.8 μA total current budget under 1.2 V, we assign about 1 μA to the AFE, while at least 800 nA to the two IAs. The amplifiers used in the IA and the PGA stage are shown in Fig. 3. The IA uses single-stage design to improve the current efficiency and reduce the thermal noise, while the flicker noise performance is optimized by using large transistors for the input pair.

3.3 Level-Crossing ADC

The level-crossing ADC in the A2I samples the ECG signal adaptively based on input activities. The amplified output from AFE \(V_A\) is continuously monitored by the two asynchronous comparators \(C_1\) and \(C_2\). Whenever \(V_A\) voltage increases or decreases one quantization level or 1/32 of \(V_{DD}\), a sample is generated representing the change. The ADC produces two delta-modulated outputs, \(DIR\) and \(REQ\). \(DIR\) represents the input voltage change direction, and each pulse at \(REQ\) represents one level-crossing event.

Due to the sporadic feature of ECG signals, the number of LC samples is typically around 10% of Nyquist-based systems, which effectively reduces the output data rate as well as the dynamic power. Therefore the static power from the asynchronous comparators and the feedback digital-to-analog converter (DAC) are the most power consuming blocks. We allocate 150 nA to each comparator with the schematic shown in Fig. 5, and about 50 nA to the DAC. The first stage of the comparator, highlighted in the gray box in Fig. 5, accepts rail-to-rail input [9]. And it does not require any extra biasing circuits. Large resistors are used in DAC array to reduce the static current.

3.4 1B2B Pulse Encoder

The 1B2B encoder converts 2 pulse streams from the A2I output to a single pulse stream for the wireless TX. The coding scheme is illustrated in Fig. 6. Every RISE event is represented by 2 narrow pulses with 400 ns interval defined through delay cells, and every FALL event is kept as a single
3.5 IR-UWB Transmitter

The wireless radio design also takes the event-driven nature into consideration. The popular choice of narrow-band transmitter using MICS/ISM band at 400 MHz is not the best solution especially for this clockless system. The targeted communication distance is limited to few centimeters for low power consideration. Narrow-band communication requires clocks and the power overhead is large for this short distance communication application.

We therefore choose the impulse-radio UWB transmitter as shown in Fig. 7. The transmitter is designed for 3-5 GHz band, which is a trade-off among antenna size, power, and selected CMOS process. As much as 1.4 µA static current is allocated to the output stage, which consists of two transistors $M_{1,2}$, to ensure adequate signal bandwidth. The digital edge-combining technique is used to generate the mono-cycle pulse while the cascade amplifier with optimized on-chip inductor is used to drive the on-chip antenna. Mono-pulse minimizes the hardware cost while it does not violate the FCC spectrum mask since the data rate is very low. The pulse width is controlled digitally ($D_0 - D_3$) by varying the load capacitance of the inverter. The TX is activated only if data pulses are received from the 1B2B encoder. In other words if the input ECG voltage does not change, the dynamic power of the system is close to zero. The heavy duty-cycling of the TX significantly reduces the power consumption, and fits perfectly in the event-driven system.

4. VERIFICATION AND MEASUREMENT RESULTS

The ECG SoC, including the AFE, A2I, 1B2B encoder, and IR-UWB, is implemented in 0.13 µm CMOS technology. To reduce device size and cost, a $2 \times 2.5$ mm$^2$ coplanar waveguide-fed monopole antenna is also integrated on chip. The die photograph as well as the evaluation board is shown in Fig. 8. Individual circuit blocks are first evaluated. The input referred noise of the AFE is 3.06 µV rms within the ECG bandwidth of 0.05 Hz to 180 Hz, as shown in Fig. 9 (a). The signal-to-noise ratio (SNR) for the front-end including the ADC is 42.2 dB, using a 10-Hz single-tone test input. Fig. 9 (b) provides the output spectrum. We also tested the A2I function using ECG captured from human subjects. Fig. 9 (c) shows the reconstructed ECG output from the A2I ADC output. The measured UWB TX’s output pulse voltage swing is 600 mV with a 50Ω load shown in Fig. 9 (d). It achieves the FCC compliance at the data rate of 100 kbps as shown in Fig. 9 (e). The de-embedded measurement of the on-chip antenna shows that it achieves -10 dB return loss from 2 to 7 GHz. The simulated radiation pattern in Fig. 9 (f) indicates an omni-directional pattern with a peak realized gain of -37.3 dBi at 4 GHz.

Next we test the complete sensor in the designed application scenario. A customized UWB receiver is built to record the pulse train from the ECG SoC. It consists of a wideband
antenna, an LNA, a pulse detector, and a digital oscilloscope as baseband to record the pulses. The receiver is placed 2 cm apart from the chip, which emulates the communication path from the sensor to the gateway device put at the T-shirt pocket. Fig. 9 (g) illustrates the pulses received by the RX, and the reconstructed signal. To capture at least two heart beats for demonstrating the wireless link, the oscilloscope is set to 1 GHz sampling rate due to available memory size. Because of low sampling rate of the oscilloscope, some pulses were missed during recording, which causes distortion in reconstructed ECG signal. The best way is to design a complete UWB transceiver for capturing the pulses from TX. This will be the future work. Table 1 summarizes the chip measurement results and comparisons with prior arts. The entire SoC consumes 2.89 µW under 1.2 V supply while transmitting raw ECG data, which is one magnitude lower than the state-of-the-art designs.

We also conduct tests to demonstrate new capabilities attained by the proposed DC-coupled AFE. The test uses dry electrodes on human subjects. With over 3.6 GΩ measured input impedance at low frequency range, the captured ECG signal is robust against interference including motion artifacts. Fig. 10 shows the chest strap and the dry metal electrodes mounted during the measurement. The outer periphery of the electrode is shielded using the input common mode \( V_{CM} = \frac{V_{DD}}{2} \) for body biasing. Two ECG traces are captured when the subject is walking and doing exercises, and plotted in Fig. 11. It is clear that the ECG baseline is stable and all vital waves are easily identifiable. In the bottom plot of Fig. 11, the heart rate is slightly higher due to the exercises, but the baseline drift remain limited and no signal clipping occurs.

This high-impedance AFE is also tested to capture ECG signal from one arm. This is not possible for most of ECG chips with limited AFE input impedance. In this test, two
Electrodes are attached on the left upper arm, with each about 4 cm apart. The captured signal is filtered to remove the 50-Hz interference, and the result is given in Fig. 12. Note even though the peak-to-peak voltage is only 0.2 mV, the heart beat peaks as well important features are still identifiable. Thanks to the DC-input AFE, the SoC is able to acquire such a small ECG signal.

5. CONCLUSION

We have proposed in this paper a ultra low-power wireless ECG SoC for ambulatory heart monitoring. The level-crossing A2I minimizes number of samples leading to significant reduction in total power consumption.

The DC-input front-end with 3.6 GΩ input impedance improves the signal quality by reducing the effects of motion artifacts and other interference. The baseline stabilizer automatically resets the front-end to avoid saturation due to DC drift. The impulse radio UWB takes the full benefits from event-driven architecture and transmits the “events” representing modulated ECG signal to a nearby gateway. The entire sensor consumes 2.89 µW while transmitting the raw ECG data. The highly integrated ECG chip does not require any external clocks, antennas, or wet electrodes, which makes it a promising candidate for cost-efficient wireless ECG patches.

6. REFERENCES